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To cite this version:


HAL Id: ensl-00610328
https://hal-ens-lyon.archives-ouvertes.fr/ensl-00610328v3
Submitted on 15 Nov 2011

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Multiplication by rational constants

I. INTRODUCTION

Multiplication by constants has received much attention in the literature, especially as many digital signal processing algorithms can be expressed as products by constant matrices. In such cases the constants are typically irrational (e.g. the square roots of unity in a Fast Fourier Transform).

The context of the present work is quite different. We are interested in porting applications into optimized architectures for FPGAs, and in this process we want to optimize the arithmetic operators when possible. Such applications often involve multiplications by rational constants, and this article studies how to implement them as efficiently as possible.

Our initial motivation was floating-point divisions by 3 and that correct rounding very often comes for free in practice.

There are three contributions in this article. We first present the previous state of the art. It is also shown that for such constants, the additional cost for a correctly rounded result is very small, and that correct rounding very often comes for free in practice.

II. ON THE PERIODICITY OF THE BINARY REPRESENTATION OF RATIONAL NUMBERS

The most usual system of representing numbers is the position system, where a number is represented by a sequence of digits,

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Index Terms—multiplication by a constant, rational number, floating-point, reconfigurable computing

Abstract—Multiplications by simple rational constants often appear in fixed-point or floating-point application code, for instance in the form of division by an integer constant. The hardware implementation of such operations is of practical interest to FPGA-accelerated computing. It is well known that the binary representation of rational constants is eventually periodic. This article shows how this feature can be exploited to implement multiplication by a rational constant in a number of additions that is logarithmic in the precision. An open-source implementation of these techniques is provided, and is shown to be practically relevant for constants with small numerators and denominators, where it provides improvements of 20 to 40% in area with respect to the state of the art. It is also shown that for such constants, the additional cost for a correctly rounded result is very small, and that correct rounding very often comes for free in practice.

Multiplication by rational constants

Multiplication by a constant, rational number,
and each digit is weighted by powers of some radix, usually 10 (decimal system) or 2 (binary system).

In such a system, any rational number \(a/b\) has an eventually periodic representation. This is true in decimal \((1/3 = 0.333\ldots, 1/9 = 0.1111\ldots)\) but also in binary \((1/3 = 0.01010101\ldots, 1/9 = 0.00111001110001\ldots)\). Numbers with a finite decimal representation can be viewed as a special case where the periodic pattern is composed of zeroes, for instance \(0.5 = 0.50000\ldots\). A number with a finite decimal representation may have an infinite binary one, for instance \(1/5 = 0.2_{10} = 0.00110011001\ldots\). The opposite is not true, due to the fact that two divides ten.

The following lemma tells us which numbers have a purely periodic binary representation:

**Lemma 1.** Let us consider an irreducible fraction \(c/d\), where 2 divides neither \(c\) nor \(d\). If \(c < d\), then the binary representation of \(c/d\) is purely periodic, i.e. it starts with an occurrence of the periodic pattern.

The condition that 2 divides neither \(c\) nor \(d\) is not a constraint, since powers of two correspond to shifts in binary. For most purposes, they may be handled separately in a trivial way. If \(c > d\) the Euclidean division of \(c\) by \(d\) gives us \(c = hd + c'\), and we may rewrite \(c/d = h + c'/d\). For the purpose of multiplying an input \(x\) by the constant \(c/d\), we therefore have \(cx/d = hx + c'x/d\). Existing literature addresses the multiplication by the finite integer constant \(h\), so we may focus on the multiplication by the purely periodic constant \(c'/d\).

The following lemma allows us to compute the periodic pattern:

**Lemma 2.** Let \(c/d\) be an irreducible fraction, where \(c < d\), and 2 divides neither \(c\) nor \(d\). The size \(s\) of its period is the multiplicative order of 2 modulo \(d\), i.e. the smallest integer such that \(2^s \mod d = 1\). The periodic pattern is the integer \(p = [2^s c/d]\).

**Proof:** By definition of \(s\) we have \(2^s = kd + 1\) for some integer \(k\). Therefore \(p = [2^s c/d] = \left\lfloor \frac{(kd+1)c}{d} \right\rfloor = k[c + c/d] = kc\) since \(c/d < 1\). We deduce that
\[
2^s c/d = p + c/d,
\]
where the recursive occurrence of \(c/d\) exactly expresses the periodicity of the fraction \(c/d\).

**Examples:**
- \(1/3\) has period size \(s = 2\) because \(2^2 \mod 3 = 1\). The pattern is \([1 \times 2^2/3] = 1\), which we write on 2 bits 01, and we obtain that \(1/3 = 0.(01)_{\infty}\);
- \(5/9\) has period size \(s = 6\) because \(2^6 \mod 9 = 1\). The pattern is \([5 \times 2^6/9] = 35\), which we write on 6 bits 100011, and we obtain that \(5/9 = 0.(100011)_{\infty}\).

Thanks to these lemmas, algorithm 1 determines the periodic binary representation of a fractional number \(a/b\). This representation consists of 4 integers:

- \(s\) the period size in bits, a positive integer.
- \(p\) the periodic pattern, a positive integer that we will usually write in binary.
- \(h\) the header, a positive integer, also typically written in binary.
- \(e\) the scaling factor exponent, or shift. Such as
\[
a/b = 2^e \left( h + \sum_{i=1}^{\infty} \frac{p}{2^{si}} \right).
\]

### Algorithm 1. Computing the periodic representation of a rational \(a/b\) as a tuple of integers \((e, h, p, s)\).

1. **procedure** \begin{unboxedequation}
\begin{align*}
P_{\text{PERIODIC\_REPRESENTATION}}(a, b) & \quad
\begin{align*}
c, d & \leftarrow \text{SIMPLIFY}(a, b) \\
e & \leftarrow 0 \\
& \quad \begin{align*}
& \text{while } c \mod 2 = 0 \\
& \quad c & \leftarrow c/2 \\
& \quad e & \leftarrow e + 1 \\
& \quad \text{end while} \\
& \text{while } d \mod 2 = 0 \\
& \quad d & \leftarrow d/2 \\
& \quad e & \leftarrow e - 1 \\
& \quad \text{end while} \\
& \quad (\text{Now } a/b = 2^e c/d \text{ with both } c \text{ and } d \text{ odd}) \\
& \quad h & \leftarrow c/d \\
& \quad c & \leftarrow c \mod d \\
& \quad h & \leftarrow c/d \\
& \quad s & \leftarrow 1 \\
& \quad \begin{align*}
& \text{if } d = 1 \quad (a/b \text{ has a finite binary representation}) \\
& \quad p & \leftarrow 0 \\
& \quad \text{else} \quad (a/b \text{ has an infinite binary representation}) \\
& \quad t & \leftarrow 2 \\
& \quad \text{while } t \mod d \neq 1 \\
& \quad s & \leftarrow s + 1 \\
& \quad t & \leftarrow 2t \\
& \quad \text{end while} \\
& \quad p & \leftarrow cd/d \\
& \quad \text{end if} \\
& \quad (e, h, p, s) & \leftarrow (e, h, p, s) \\
& \quad \text{return} \\
& \quad \text{end procedure}
\end{align*}
\end{align*}
\end{unboxedequation}

### III. PERIODICAL SHIFT-AND-ADD TREES

In this section, we input the periodic representation of a rational constant \(a/b\), and also a precision \(w_0\), which is the number of bits of \(a/b\) that have to be considered for the multiplication. The value of \(w_0\) typically expresses the accuracy requirements of the floating-point or fixed-point context. For instance, section IV will define the value of \(w_0\) that ensures correct rounding for a given floating-point format.

In [5], Gustafsson and Qureshi suggested trying to represent a real constant on more than \(w_0\) bits if it leads to a shift-and-add architecture with fewer additions. They indeed mention the
fact that, due to their periodic representation, rational constants are good candidates for exploiting this idea, without exploiting this idea systematically.

With the notations of previous section, let us define

$$\pi_0 = 2^{-s} px.$$ 

The $2^{-s}$ factor simply scales the integer $p$ to an approximation of $c/d < 1$, so $\pi_0$ is an approximation of $c x/d$. We may then compute increasingly accurate approximations of $c x/d$ as

$$\pi_1 = \pi_0 + 2^{-s} \pi_0,$$

$$\pi_2 = \pi_1 + 2^{-2s} \pi_1,$$

and in general

$$\pi_{i+1} = \pi_i + 2^{-2^s} \pi_i,$$

so that $\pi_i$ is the product of $x$ by an approximation of $c/d$ of size $2^i s$ bits.

Therefore, a constant corresponding to $2^i$ repetitions of the period may be built in $i$ additions, and this is optimal [6].

Let us now consider the details, including further optimizations. We note $w_h$ the size in bits of the header $h$. We need to compute $h x + c x/d$, where $c x/d$ is the periodic part. If $w_0$ is the precision to which $h + c/d$ must be represented, then $c/d$ must be represented at least on $w_0 - w_h$ bits.

First, one of the existing methods is used to build $p x$ and, if $h \neq 0$, $h x$. As these two constants should be small for the method to be relevant, exhaustive exploration techniques [9], [10], [12] may be used to perform this step optimally. Such methods lead to less than 4 additions for any $h$ or $p$ of size smaller than 12 bits, and less than 5 additions for sizes smaller than 19 bits. The FloPoCo implementation currently uses the simpler heuristic presented in [14], which is better suited to hardware as it also minimizes the size of the adders and leads to minimum-depth adder trees. In our experiments, it consistently computes a minimal-adder-count architecture, probably due to the fact that both $h$ and $p$ are very small integers for the simple rationals that motivate this work.

Then we may compute the $\pi_i$. In this process, we may stop as soon as $2^i s \geq w_0 - w_h$. However, it is usually possible to implement a smaller last addition. Let $i$ be such that $2^i s < w_0 \leq 2^{i+1}s$: we must compute the $\pi_j$ for $0 \leq j \leq i$. Let $j$ be the smallest integer such that $(2^i + 2^j)s \geq w_0 - w_h$. As $j \leq i$, $\pi_j$ is already computed, and the last stage may compute

$$f = \pi_j + 2^{-2^i s} \pi_i$$

(another option would be to compute $f = \pi_i + 2^{-2^i s} \pi_j$, but this would lead to a larger adder [14]).

If $h = 0$, this is all. If $h \neq 0$, we still have to add $h x$. This product is itself computed using a classical constant multiplier, in parallel to the computation of the fractional product. There are two possible parenthesing of the two final additions: $r = (h x + \pi_j) + 2^{-2^i} \pi_i$ or $r = h x + (\pi_j + 2^{-2^i} \pi_i)$. We may assume that the computation of $h x$ has a depth strictly smaller than that of $\pi_i$ (which should be the case for “small” rationals).

With this assumption, as soon as $j < i$, the first parenthesing leads to a shallower tree, and is therefore preferred. If $i = j$,

the second parenthesing will be preferred when it leads to a smaller overall number of full adders.

Figure 1 illustrates the resulting architecture on the example of $a/b = 7/5$ for single precision, with a target precision $w_0 = 28$ (providing correct rounding according to Section IV). The smallest value of $i$ such that $2^i s \geq 28$ is $i = 3$. We don’t find in this case a smaller $j$ such that $(2^i + 2^j)s \geq 28$. For this simple example the product $p x$ is computed in one addition only, while the product $h x$ is computed in zero additions.

This figure also illustrates a small additional optimization: we trim, whenever possible, leading and trailing zeroes from the various sub-constants to minimize datapath width. For instance, for $a/b = 7/5$, the period is $p = 01102$, but $\pi_0$ is actually computed as $x \times 112$ and the two zeroes are added only when performing the shifts. The final result is actually one bit more accurate than it seems, since there is one more trailing zero to the truncated constant. These technical details are taken into account by the generator in FloPoCo.

IV. CORRECT ROUNING

It turns out that for the small rational constants for which this method is of interest (“small” meaning small $a$ and small $b$), obtaining a correctly rounded result is also fairly cheap. More specifically, the following theorem holds. It is, in essence, a generalization of the “exclusion lemma” used to prove that some division algorithms are correctly rounded [18].

Theorem 1. Let $n$ be the precision of the input $X$ and $q$ be the precision of the result $R$, and assume $q \geq n$. If $C$ is a constant obtained by truncating the binary representation of $a/b$ to at least $q + 1 + \lceil \log_2 b \rceil$ bits, then rounding the product $C X$ to the nearest floating-point number of precision $q$ is equivalent to rounding the exact product $a/b X$.

Note that this theorem covers the most useful case when the input and output precisions are identical.
Fig. 2. The KCM LUT-based method

\[ X = X_0 + 2^{-a}X_1 + 2^{-2a}X_2 + 2^{-3a}X_3 \]
\[ CX = \begin{array}{cccc}
X_0 & X_1 & X_2 & X_3 \\
+CX_0 & + & + & + \\
+ & + & + & + \\
\end{array} \]
\[ \begin{array}{c}
q + g \\
\end{array} \]

and we have a sum of (shifted) products \( CX_i \). Instead of computing these products, we read \( CX_i \) from a table of pre-computed values \( T_i \), indexed by \( X_i \).

The cost of each table is one FPGA LUT per output bit (on Figure 2, the corresponding boxes are sized accordingly).

We also have to count the cost of computing the sum of these \( CX_i \). The minimal cost is obtained with the sequential implementation of this sum depicted on Figure 2: it consists of \( \lceil n/\alpha \rceil - 1 \) adders of increasing sizes. However, an adder tree, reducing the latency for a slightly larger overall cost, is usually preferred. As the cost of an adder in FPGAs is typically one LUT per bit, the cost of the adders is roughly equivalent to the cost of the tables.

The FixRealKCM operator in FloPoCo implements this technique. In addition, to ensure last-bit accuracy of \( CX \), the datapath has to be extended with \( g \) guard bits that will absorb the rounding errors performed when filling the tables [19]. The error analysis determining \( g \) is easily adapted to ensure correct rounding in the case of rational constants, using the results of Section IV.

We now remark that the periodicity of the constant also leads to an optimization of the KCM tables. To illustrate it, let us take as an example \( C = 1/3 \), and consider in Figure 3 a table holding \( X_i/3 \) for \( X_i \) on \( \alpha = 4 \) bits. Since each row, having the same denominator, is eventually periodic, the whole table is eventually periodic. This example 22-bit table can be implemented as 5 LUTs instead of 22. In general, for a constant \( a/b < 1 \) of period size \( s \), the table for \( a/bX \), requires of the order of \( 2^s \) LUTs: only the most significant \( \alpha \) bits are not periodic.

This optimization only reduces the size of the tables, not the size of the adders, which limits its impact to a 50% improvement at most. However, it is discovered by synthesis tools, so we do not need to explicit it in the code.

VI. RESULTS AND COMPARISONS

Table I provides some results obtained thanks to FloPoCo for the proposed multipliers, compared to the previous implementation of [14], and (for FPGAs) to the KCM approach. In the latter case, one Logic Element (LE) may implement one 4-input LUT, or one Full Adder (FA): the costs reported on each line indeed use the same units.

In all the cases of Table I, the previous shift-and-add approach from [14] already builds a tree of optimal depth, but not of optimal size. Specifically, it does build sub-constants which are repetitions of the period, but the numbers of repetition are not always powers of two, which prevents reusing them optimally. The same holds for the implementation of [9] on spiral.net.
It could be interesting to study if variations of this technique to a correctly rounded divider by a multiplier by \(\alpha\) technique is the implementation of divisions by small integers.

The periodic binary representation of rational constants can be usefully exploited to build efficient hardware for the multiplier by such constants. An implementation of this idea in the open-source FloPoCo core generator is demonstrated. This approach still wins, and KCM is only interesting for precisions smaller than 24 bits.

The KCM approach leads to an adder count proportional to the input precision \(n\) and independent of the constant. However, most of these adders are smaller than the output precision \(q\) (see Figure 2), whereas the adders in the shift-and-add method are all larger than \(n\) (see Figure 1). Therefore, KCM is competitive for small \(n\) (typically smaller than 20) especially if \(q > n\) [19].

The KCM results are given for \(\alpha = 4\) for comparison with the literature (for instance [16] reports 308 LUTs for a KCM with a 24-bit input and a 24-bit constant – this would not even offer correct rounding as the operators of Table I). However, recent FPGAs have larger LUTs (\(\alpha = 5\)), which leads to a typical reduction of 4/5 of the KCM cost. In our table, a KCM with \(\alpha = 5\) would take the lead only for the first line (113 LE instead of 127 for KCM with \(\alpha = 4\), and 118 LE for the periodic shift-and-add). For the other lines, the shift-and-add approach still wins, and KCM is only interesting for precisions smaller than 24 bits.

VII. Conclusion

The periodic binary representation of rational constants can be usefully exploited to build efficient hardware for the multiplication by such constants. An implementation of this idea in the open-source FloPoCo core generator is demonstrated. This technique is mostly relevant for constants \(a/b\) where both \(a\) and \(b\) are small integers, and in this case correct rounding of the multiplication by the infinitely accurate rational constant comes at a minor overhead: On most of the examples studied, correct rounding is for free. An important application of this technique is the implementation of divisions by small integers. A multiplier by \(1/b\) using this approach is bit-for-bit equivalent to a correctly rounded divider by \(b\).

It could be interesting to study if variations of this technique could not be used to implement division by small integers in software multiple-precision packages.

TABLE I

| \(\alpha\) | \(\beta\) | \(\gamma\) | \(\delta\) | \(\epsilon\) | \(\zeta\) | \(\eta\) | \(\theta\) | \(\iota\) | \(\kappa\) | \(\lambda\) | \(\mu\) | \(\nu\) | \(\xi\) | \(\omicron\) | \(\pi\) | \(\rho\) | \(\sigma\) | \(\tau\) | \(\upsilon\) | \(\phi\) | \(\chi\) | \(\psi\) | \(\omega\) |
| 1/3 | 24 | 32 | 4 (118) | 27 | 4 (190) | 5 (127) | 24 | 24 | 113 | 128 | 6 (192) | 54 | 28 | 193 | 24 | 12 (613) | 33 | 5 (139) | 53 | 6 (266) | 57 | 6 (395) | 12 (394) |
| \(h = 0\) | \(p = 0.11_2\) | \(19\) | 24 | 30 | 5 (122) | 29 | 5 (131) | 5 (167) | 115 | 120 | 7 (885) | 118 | 7 (1110) | 27 (2253) | 129 | 7 (590) | 117 | 7 (1507) | 27 (2267) |
| \(h = 0\) | \(p = 0.00111_2\) | \(75\) | 24 | 33 | 5 (139) | 28 | 5 (192) | 5 (162) | 115 | 120 | 7 (900) | 117 | 7 (1507) | 27 (2267) | 129 | 7 (590) | 117 | 7 (1507) | 27 (2267) |

Acknowledgements

Thanks to B. Pasca and A. Plesco for bringing up this question, to N. Brisebarre for his lights on number theory, and to the anonymous reviewers for their insightful suggestions.

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